

The Versatile Acquisition System of Giano

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ABSTRACT

Giano is an infrared (0.9-2.5 μm) cross-dispersed echelle spectrometer designed to achieve high throughput, high resolving power, wide band coverage and high accuracy. *Giano* will be a common user instrument which will be permanently mounted at the Telescopio Nazionale Galileo (TNG), located at Roque de Los Muchachos Observatory (ORM), La Palma, Spain.

Giano successfully concluded the development phase, and we present here some of the solutions adopted in the focal plane electronics, which take care of detector control and data acquisition and handling.

Keywords: Spectroscopy, Software, Electronics, acquisition systems

1. INTRODUCTION

Giano is an optimized near infrared spectrograph which can yield, in one shot, 0.9-2.5 μm spectra either at low ($R \simeq 400$ with a 1" slit) or high (up to $R=46,000$ with a 0.5" slit) resolutions maintaining, in both modes, a very high throughput on the whole spectral range. The detector is a Rockwell HAWAII2, 2048^2 $18\mu\text{m}$ pixel with PACE FPA. This instrument will be the result of a project belonging to the Second Generation Instrumentation Plan of the Telescopio Nazionale Galileo (TNG, La Palma, Spain). *Giano* will be installed at Nasmyth B focus of TNG.

2. ARCHITECTURE

The struggle for the highest optical efficiency in *Giano* design^{1,2} can become ineffective if the acquisition system is not at the same excellence level. If read-out noise is higher than intrinsic image noise, if image acquisition and storage take a time comparable to the exposure time, or the cross-talk between quadrants is high and uncorrectable, a perfect optical system is of no use.

We derived from the Fasti project^{3,4} the general framework. In particular we stress the importance to have a *light* electronic system, which is modular, flexible and extendible. The design guideline, inherited from Fasti, are:

- to divide the system in several *modules* with clear boundaries.
- to use, as far as possible, commercial parts at board level.
- to use largely accepted standards as boundaries, as a PCI bus, an industrial standard PC104 bus or an Ethernet connection.
- to design the custom parts as concepts, not around a particular electronic device, so that they could be implemented by components from different manufacturers, or by devices developed in the future.
- to be as flexible as possible on waveform generation.

In this framework we can conceptually divide *Giano* controller into five main parts:

The pre-amplifier This part gets the detector output signal and performs both an impedance adaptation and a first amplification. This part is located inside the cryogenic enclosure at liquid nitrogen temperature.

The sequence generator This part generates all the complex clocking signal necessary to get a [sub-]frame from detector. In this part we also generate the biases and the very stable DC lines to the detector and we adapt the logical clock level to the CMOS level needed by HAWAII2.

The data conversion system This part contains the sample-and-holds and the analog to digital converters.

The data collection system This part collects the data coming from the ADCs, stores and rearranges them frame-wise.

The global controller This part coordinates all operations, performs initializations and acts as the bridge to the higher level controlling software. Here we also collect, label and transmit scientific data to the middle-ware software.

This structure gives us the maximum of flexibility. We give here only some examples of the possibilities of this approach.

- The sequence generator can be implemented by two different approaches. The first one, the SVB, is the same used for the Nics 1024² HAWAII detector: the adaptation was only a matter of changing its program file. The second one, has been already successfully used to clock a very fast optical detector, the Marconi LLLCCD.⁵ More details can be found later on.
- We will use only the four quadrant mode of the HAWAII2 detector, but the upgrade of the acquisition system to the use of all the 32 data outputs is only a matter of manufacturing more data conversion boards and wiring them to the data collection system.
- The global controller is seen from the outside as an Ethernet socket, with a packet protocol, imposing no constraints to the higher level control system architecture.

3. CLOCK GENERATION

During the installation of Fasti for Nics, we found really handy the possibility, offered by Fasti controller, to change, on the fly, the controlling waveforms for the detector. With this possibility we could be able to tune the internal delays in order to minimize the effect of non-uniformity of bias on dark frames.

For Giano controller we will use two different clock generators: The first is based on a custom micro-controller we developed for Fasti (patent FI 2004 A 000007), which can give the maximum flexibility, and will be used during the development phase, the second, based on a programmable succession of elementary waveform fragments, will be less resource-hungry and faster, and will be used on the final version of controller.

The first clock generator, named SVB and inherited from Fasti³ is based on a custom-made micro-controller, developed in-house, whose pseudo-assembler enable the direct control of level and timings of signal over an 8 bit digital bus. This pseudo-assembler gives the possibility to modify on-the-fly the waveforms. With this flexibility we can explore different detector clocking schemes, and fine-tune all details of detector operation. If adopted also at the telescope, this system allows flexible operations, as the fast switching between normal integration and *idle* integrations to remove detector memory effects, or the acquisitions (within the limit of the detector clock limits) of multiple sub-areas, even with different detector integration times. This SVB clock generator is a *conceptual design* and now is implemented on 50.000 gates of programmable logic.

We have developed a full set of software support tools for the SVB, including a pseudo-assembler compiler, an emulator and a logical-analyzer-like waveform display and exploration tool (see figure 3). The full set of documentation for these tools is available at Fasti web site, <http://www.arcetri.astro.it/irlab/fasti>.

The great flexibility of this clock generator come at the price of a steep learning curve and therefore we have developed a second solution, more apt to telescope experimentation. This second generator uses an already adopted approach and can conceptually be considered as a *macro executor*.

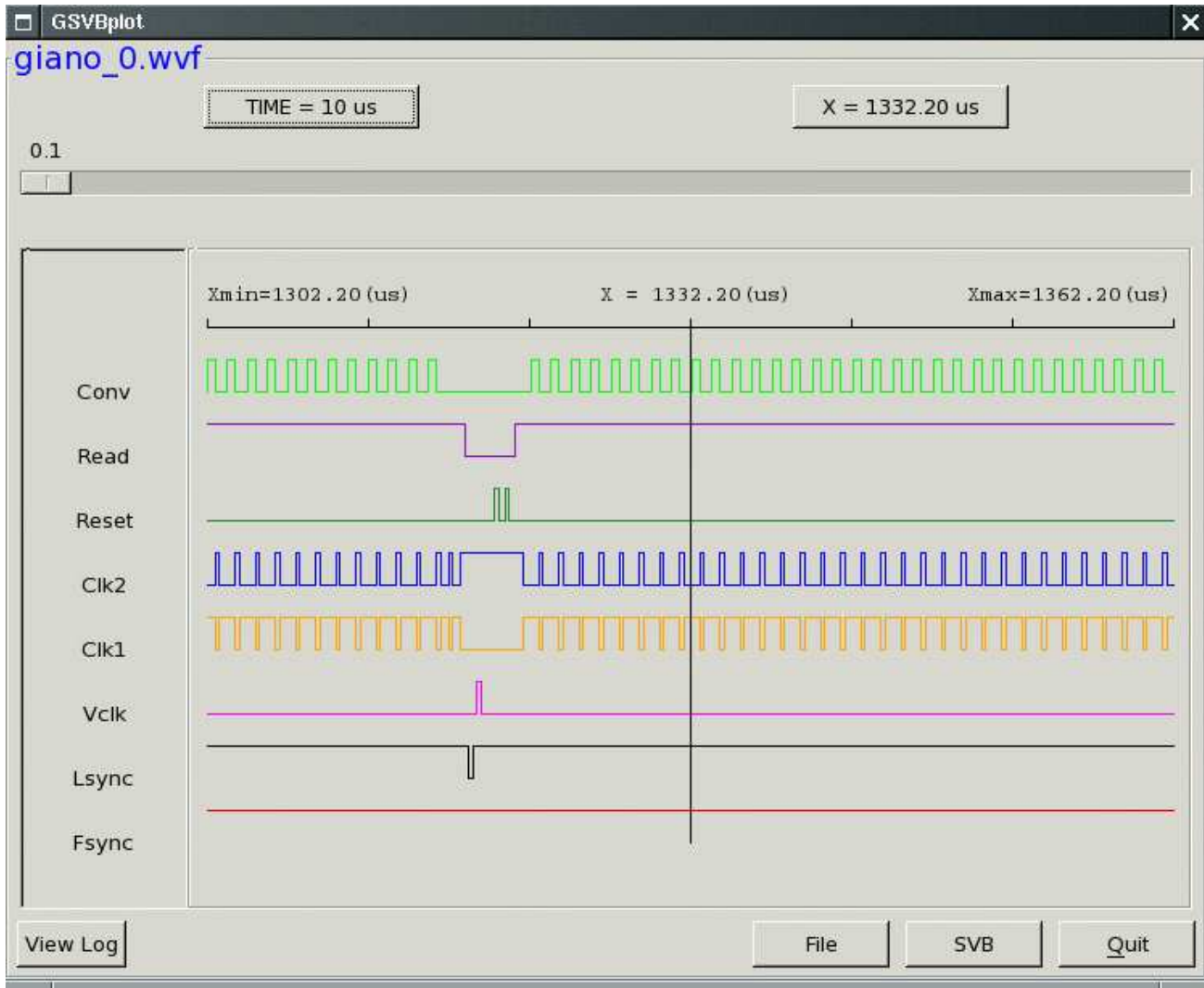


Figure 1. The waveform exploration tool for the SVB wave generator

We describe this waveform macro executor from the user point of view, while the real implementation is a program written for a programmable logic chip. Each macro comes from the division of the complex HAVAI2 waveform in many small elementary parts, each executing a limited number of operations, as the pixel read, the row increment, a single line reset and so on. There is a (ram-based) table in which each cell contains the macro type and the repetition count. The system scans the table, executing the required numbers of each waveform section, until it encounters a *restart* marker. By this approach the modification of a standard parameter as the clock scan frequency or the detector integration time (DIT) is a matter of changing numerical entries in this macro table. Also this system allows flexible telescope operations, but with less flexibility and requiring a longer preliminary test phase.

4. PRE-AMPLIFICATION

Giano aims to the maximum sensitivity at a resolving power which is quite high for an infrared spectrometer.⁶ To achieve such a result we need the lowest possible read-out noise, and, consequently, we choose to develop a custom pre-amplifier based on a very low noise discrete FETs, and to place such electronic portion as close as possible to the detector, which means within the cryogenic circuitry, inside the instrument dewar.

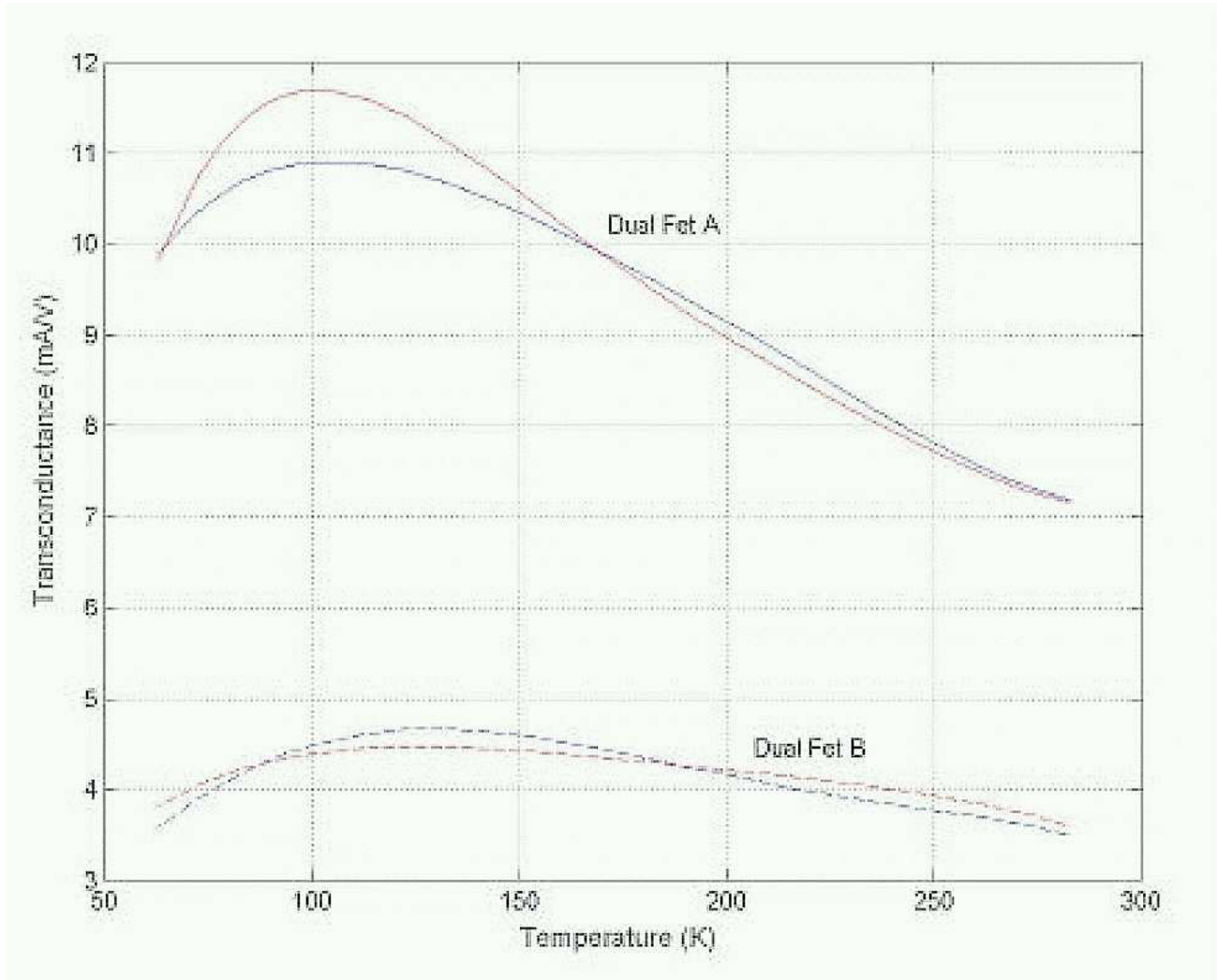


Figure 2. Transconductance versus temperature for two different JFET matched pairs.

This design substitutes the usual solution of a JFET acting as an impedance adapter in the source follower configuration with a definite gain, both in terms of signal and in term of impedance on the same board which hosts the detector on the focal plane. The amplified result is then transmitted to the external amplifier board, with a clear gain in terms of pick-up of external noise.

This choice is the same adopted in the ESO's IRACE,⁷ but with an important difference in design. While IRACE use integrated CMOS operational on the cryogenic board, we choose to utilize as front-end a discrete JFET matched pair, losing some bandwidth but gaining in intrinsic noise terms.

We selected some JFET type with very low noise and measured their characteristics at various temperatures. JFET noise is proportional to $\sqrt{T/G_m}$, where T is the temperature, in Kelvin and G_m is the transconductance, so we need to monitor the G_m variation at cryogenic temperatures. The selection process and all measures are described in Biliotti et al.⁸

We found that some devices exhibit a very favorable relationship between temperature and transconductance. This happens in a temperature range which is comfortably near the detector working temperature, but still brings to the necessity to actively control the JFET case temperature. Also some form of shielding could be necessary not to pollute the detector with the infrared glow from warmer surfaces. While the transconductance of selected

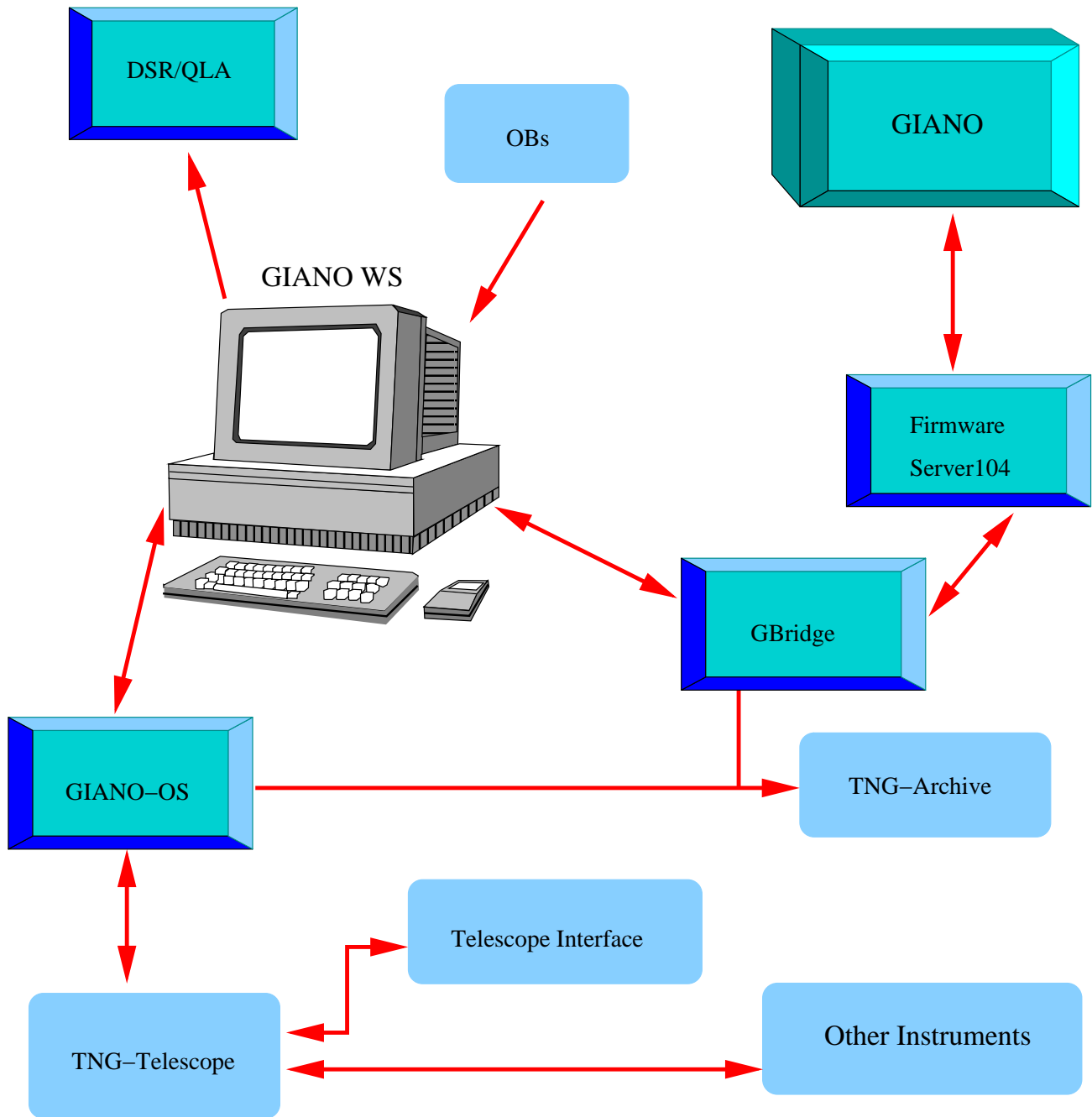


Figure 3. User perspective of Giano Software

device gives a low noise, also measurements of frequency response of the resulting pre-amplifier is suitable for conversion speed in excess of 1 MHz, giving large room for normal astronomical operations.

5. DATA ACQUISITION AND TRANSFER

Analogous data came from the cold board with some amplification and an higher impedance. However to avoid noise pick-up both on the clocking lines and on the analog signal lines, the maximum amount of care should

be taken. We provided the shortest path from detector to the external electronic board by bending the the nearest vessel wall and placing the A/D boards just outside the hollow surface.

To further improve the connection in terms of low impedance and ground shielding, we developed a particular form of connection, called FlexConnect (patent pending).

The warm electronics is composed by four boards hosting the clock generation circuitry, the analog to digital converter, a small memory buffer and a serial adapter to the LVDS bus connecting to the data buffer board.

All digital circuitry of this board is implemented inside a field programmable gate array, giving us the possibility to test various configurations. For instance we can change the clocking engine in few minutes.

We designed the prototype of this board with both a 500kHz 18 bit ADC and a faster 4MHz 16 bit ADC, from Analog devices. We tested both configuration, getting one conversion from the 18 bit and averaging 8 measurements of the 16 bit with all computations implemented in the FPGA. To our surprise, the 18 bit converter proved itself less noisy by a fair amount than its competitor and so was chosen for the final configuration.

The data generated by the ADC are transferred, by means of a serial LVDS bus to the data buffer board. The four LVDS buses are hosted on fiber optic links to minimize grounding and noise problems.

The data buffer is located near the global controller. In this board data are stored and rearranged in the natural frame format. Also in this board all the logic is realized by means of a FPGA. This board is connected to the global controller by means of a standard bus. In the prototype this bus is the PC104 industrial bus, while in the telescope version the bus will be an industrial version of the PCI standard bus.

The global controller is an embedded processor board, equipped with a custom version of the Linux Operating system. We use an industrial board, in the prototype a PC104, equipped with a passively cooled Vortex86 CPU. The operating system and the application software is located in a solid state flash memory. The 100MHz Ethernet link gives us ample bandwidth to transfer data even at the fastest acquisition rate.

6. LOW LEVEL SOFTWARE

The low level software is divided in two interacting program, Gbridge and Server104. These two programs cooperate in order to control the data acquisition system. Gbridge and Server104 runs on different systems and communicate by means of two standard TCP/IP sockets, the first for commands and messages, the second for data transfer. Both programs run as daemons and implement a client-server working model. This approach gives us all the flexibility and the debug capability we need. All communications between the two programs and the Graphical User Interface use a packet format, uniform on all channels, with acknowledge and checksum mechanisms.

Gbridge is in reality a *middle-ware* component and runs on the Giano workstation. Its role is to interpret the middle level command coming from the User Interface and to translate them into simple, low level commands, to be executed by the lower software layer (Server104). Gbridge also receives the data from the global controller and stores them in standard FITS files. Gbridge coordinates data acquisitions operation sequence and performs a logical validation on commands received. Being a daemon, in normal operation Gbridge communicates with the user interface by means of a standard socket. For testing purpose we have developed a graphical interface (Guilab) which can give all the usual command to Gbridge and can perform various data acquisition operations, from the simple one-shot integration to the continuous acquisition and display (free-run). Guilab is based on GTK-widget set.

Inside the global controller runs an operating system which is a modified of a standard CDROM Linux distribution (SLAX). At start-up this embedded operating system launches the Server104 daemon. This daemon at first takes care of the hardware auto-test and initialization, then it enters in the normal operation loop, and, after a small delay, it executes continuous no-conversion integrations to clean the array from memory effects (called dummy integrations). Upon receiving a command, as the execution of an integration, the daemon halts the dummy integrations and reprograms accordingly the sequence generator. Laboratory measurements show the small overhead introduced by the buffer read/data transmission operations.

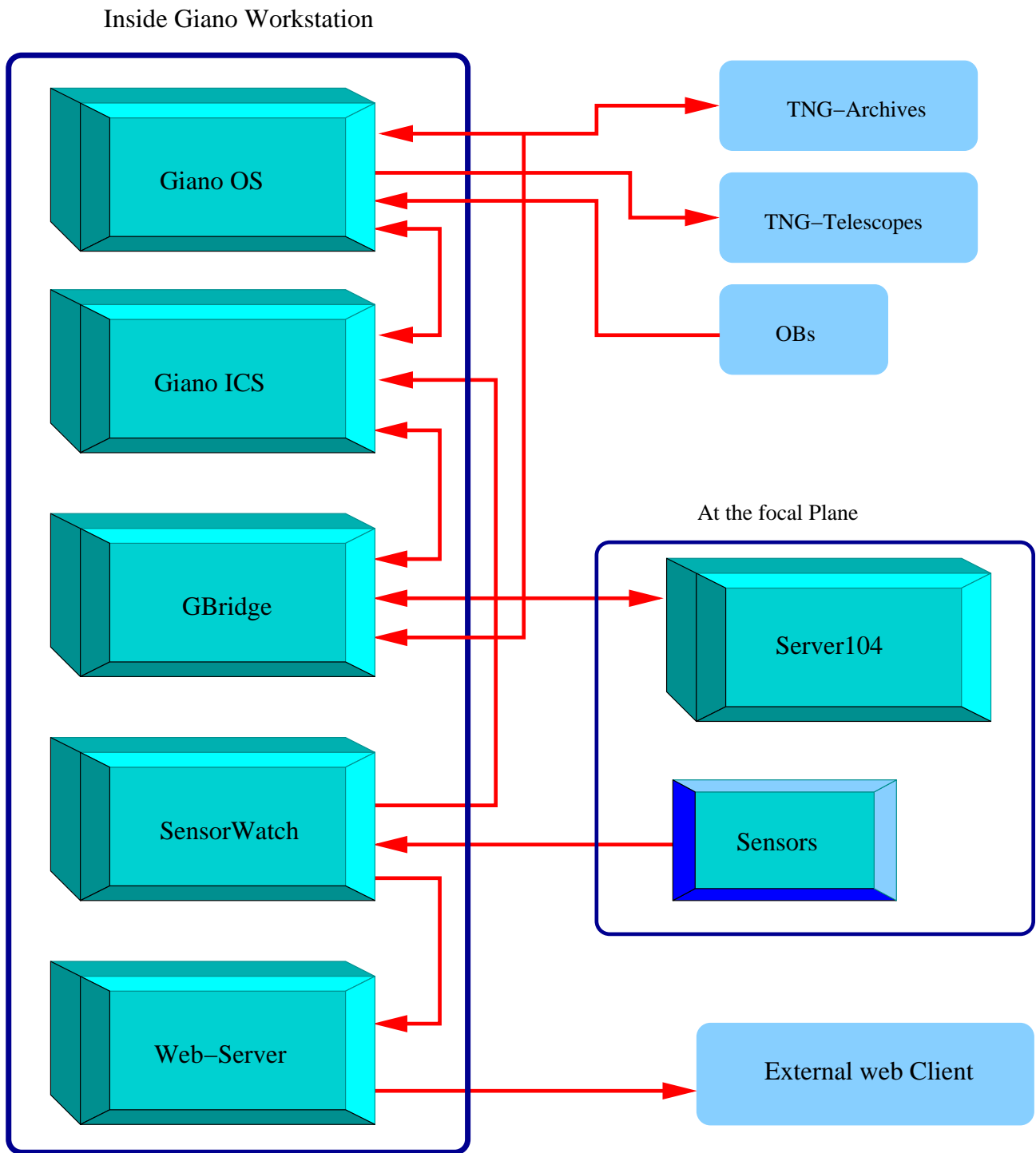


Figure 4. Structure of low-level software

Server104 also performs a continuous check of the health status of the acquisition hardware. In the controller design many auto-checks and test operations has been introduced, so the global controller can quickly recognize an error or a faulty condition and perform the appropriate operation, as to switch off detector power, or to issue an appropriate error or a warning message to the higher level software.

Also Server104 has a technical interface for laboratory testing and debug purposes. This time the interface is based on the lighter curses library, because the program runs from a small flash disk on a slow CPU (166MHz in the prototype).

7. PRESENT STATUS

The Giano acquisition system is now in the prototype phase, with all major components already working or in the finalization phase. We already acquired some images from a PACE multiplexer, and we plan to have a complete and working system by the end of the year.

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REFERENCES

1. S. Gennari, C. D. Vecchio, I. Mochi, E. Oliva, L. Origlia, F. Rossettini, R. Tomelleri, D. Milani, M. Liffredo, and G. Roveta, "The mechanics and cryogenics of giano-tng," in *this SPIE conference, paper 6269-147, Proc. SPIE*, 2006.
2. E. Oliva, L. Origlia, C. Baffa, V. Biliotti, P. Bruno, F. D'Amato, S. L. Donati, G. Falcini, S. Gennari, F. Ghinassi, E. Giani, M. Gonzalez, F. Leone, M. Lolli, M. Lodi, R. Maiolino, F. Mannucci, G. Marcucci, I. Mochi, P. Montegriffo, E. Rossetti, S. Scuderi, and M. Sozzi, "The giano at tng spectrometer," in *this SPIE conference, paper 6269-46, Proc. SPIE*, 2006.
3. C. Baffa, "The Fasti Project," *Memorie della Societa Astronomica Italiana* **74**, pp. 165–168, 2003.
4. C. Baffa, V. Biliotti, A. Checcucci, S. Gennari, E. Giani, F. Lisi, V. Gavriousssev, M. Sozzi, and G. Marcucci, "The Fasti Project," in *ASP Conf. Ser. 295: Astronomical Data Analysis Software and Systems XII*, H. E. Payne, R. I. Jedrzejewski, and R. N. Hook, eds., pp. 355–358, 2003.
5. I. Foppiani, C. Baffa, V. Biliotti, G. Bregoli, G. Cosentino, E. Giani, S. Esposito, B. Marano, and P. Salinari, "Photon counting CCDs as wavefront sensors for AO," in *Adaptive Optical System Technologies II. Edited by Wizinowich, Peter L.; Bonaccini, Domenico. Proceedings of the SPIE, Volume 4839, pp. 312-316 (2003).*, P. L. Wizinowich and D. Bonaccini, eds., pp. 312–316, Feb. 2003.
6. E. Oliva, L. Origlia, R. Maiolino, S. Gennari, V. Biliotti, E. Rossetti, C. Baffa, F. Leone, P. Montegriffo, M. Lolli, F. D'Amato, P. Bruno, S. Scuderi, F. Ghinassi, M. Gonzalez, M. Lodi, G. Falcini, E. Giani, G. Marcucci, and M. Sozzi, "GIANO: an ultrastable IR echelle spectrometer optimized for high-precision radial velocity measurements and for high-throughput low-resolution spectroscopy," in *Ground-based Instrumentation for Astronomy. Edited by Alan F. M. Moorwood and Iye Masanori. Proceedings of the SPIE, Volume 5492, pp. 1274-1279 (2004).*, A. F. M. Moorwood and M. Iye, eds., pp. 1274–1279, Sept. 2004.
7. G. Finger, R. J. Dorn, M. Meyer, L. Mehrgan, J. Stegmeier, and A. F. M. Moorwood, "Performance of large-format 2Kx2K MBE grown HgCdTe Hawaii-2RG arrays for low-flux applications," in *Optical and Infrared Detectors for Astronomy. Edited by James D. Garnett and James W. Beletic. Proceedings of the SPIE, Volume 5499, pp. 47-58 (2004).*, J. D. Garnett and J. W. Beletic, eds., pp. 47–58, Sept. 2004.
8. V. Biliotti, E. Oliva, S. Gennari, C. Baffa, G. Falcini, E. Giani, I. Mochi, and M. Sozzi, "Characterization of fets at cryogenic temperatures and its implications on the design of ultra-low noise pre-amplifiers for infrared focal plane arrays.." Submitted to *Astronomy & Astrophysics*, 2006.